國立東華大學

課　　綱　Course Outline

資訊工程學系國際組

中文課程名稱 Course Name in Chinese	數位邏輯設計實驗				
英文課程名稱 Course Name in English	Digital Logic Design Laboratory Experiments				
科目代碼 Course Code	CSIEB0110	班 別 Degree	學士班 Bachelor’s		
修別 Type	學程 Program	學分數 Credit(s)	1.0	時 數 Hour(s)	1.0
先修課程 Prerequisite					

課程目標
Course Objectives

At the completion of the course, students can design digital circuit through practical experiments. The experiments include basic logic gates, combinational logic circuits, and sequential logic circuits.

系教育目標
Dept.’s Education Objectives

1	具備學科知識，養成專業技能 Acquire academic knowledge, develop professional skills
2	學習創新思考，分析解決問題 Inspire innovative thinking, increase analytical problem solving ability
3	培養團隊精神，學習溝通合作 Promote teamwork spirit, encourage coordination and cooperation
4	提昇專業倫理，承擔社會責任 Sublimate professional ethics, engage social responsibility
5	涵育人文素養，開拓國際視野 Cultivate humanities, broaden global perspectives

	系專業能力 Basic Learning Outcomes	課程目標與系專業能力相關性 Correlation between Course Objectives and Dept.’s Education Objectives
A	資訊專業終身學習能力 Ability of lifetime learning in information profession	●
B	實驗驗證資訊科學能力 Ability of validate experimental result validation in information science field	●

C	資訊工具整合運用能力 Ability of integrated applications of information technology	●
D	資訊系統應用設計開發能力 Ability of information application system design and development	○
E	團隊合作溝通協調能力 Ability of teamwork, communication, and coordination	●
F	資通訊科技問題解決能力 Ability of problem solving regarding information and communication technology	○
G	瞭解資訊科技多元影響能力 Ability to understand information technology’s multiple influences	
H	肩負資訊人社會責任能力 Ability of bearing the social responsibilities being among information professionals	

圖示說明Illustration ：● 高度相關 Highly correlated ○中度相關 Moderately correlated

課程大綱
Course Outline

1. Introduction for specifications of TTL and CMOS ICs.
2. Introduction for Quartus II and FPGA platform.
3. Implementation of a circuit based on Encoder/Decoder and 7-segment display.
4. Implementation of BCD Adder.
5. Implementation of Counter and Frequency Division Circuit.
6. Implementation of parallel-to-serial circuit based on Mux and Demux.
5. Implementation of S-R, J-K, T, and D type flip-flops using Verilog and Altera DE2-70.
7. Redo previous experiments by using Verilog and Altera DE2-70.
7. Design example: seven segment display
8. Design example: code converter

資源需求評估（師資專長之聘任、儀器設備的配合・・・等）
Resources Required (e.g. qualifications and expertise, instrument and equipment, etc.)

Quartus II and FPGA platform*20 & PC

課程要求和教學方式之建議
Course Requirements and Suggested Teaching Methods

1. 分組實作Group experimental
2. 同儕輔導Peer tutoring
3. 助教協助實驗操作TA assist in experimental operation

其他
Miscellaneous